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A CMOS SPAD Line Sensor with per-pixel Histogramming TDC for Time-Resolved Multispectral Imaging

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Abstract—A 512×16 single photon avalanche diode (SPAD) based line sensor is designed in a $0.13 \mu\text{m}$ CMOS image sensor technology for time resolved multispectral beam scanned imaging. The sensor has $23.78 \mu\text{m}$ pixel pitch and incorporates one SPAD array with 49.31% fill factor optimized for detection in the blue-green spectral region, and a second array at 15.75% fill factor optimized for the red-NIR spectral region. Each pixel contains a 32-bin histogramming time-to-digital converter (TDC) with a mean time resolution of 51.20 ps. Histogram bin resolutions are adjustable from 51.20 ps to 6.55 ns per bin. The line sensor can operate in single photon counting (SPC) mode (102.1 giga-events/s), time-correlated single photon counting (TCSPC) mode (192.4 million-events/s) or on-chip histogramming mode (16.5 giga-events/s), increasing the count rate up to 85 times compared to TCSPC mode. Sensor capability is demonstrated through spectral fluorescence lifetime imaging, resolving three fluorophore populations with distinct fluorophore lifetimes.

Index Terms—CMOS, Histogramming, Fluorescence lifetime imaging microscopy (FLIM), single photon avalanche diode (SPAD), single photon counting (SPC), time-correlated single photon counting (TCSPC), Time-resolved spectroscopy.

I. INTRODUCTION

CMOS SPAD technology enables massively parallelized counting and timing of single photons in imaging, line and single point sensor formats [1]. The per-pixel time-resolution or gating offered by SPAD line sensors opens up new applications in hyperspectral scanning systems in microscopy, endoscopy and aerial monitoring as well as new modalities in ring-down, fluorescence lifetime and Raman spectroscopies [2]–[6]. Monolithic on-chip integration of SPADs with complex digital processing circuits implemented in standard deep sub-micron CMOS enables rich and high performance functionality to be

achieved. Several architectures have been explored in the literature including gated counters [2], time-gated memories [4], in-pixel center-of-mass computation [5], [6], per-pixel time-to-digital converters (TDCs) [3], column parallel flash TDCs [7], multi-event folded flash TDCs [8], off-chip FPGA TDCs [9], and on-chip histogramming [10], [11].

Time-correlated single photon counting (TCSPC) [12] is the most photon-efficient technique for measuring fluorescence lifetime in the time-domain [13]. It is performed by repeatedly timing fluorescence emission with respect to a synchronized pulsed optical excitation, to build a histogram of the lifetime decay. However, a major limitation of this technique is the restrictively low photon arrival rate that is well below 10% of the excitation rate, which is necessary in order to avoid distortion of the decay histogram due to pile-up [14] caused by both long detector dead-time and the inability of the TDC to process more than one event per excitation period [15], [16]. Integrated TCSPC arrays based on CMOS SPADs offer significant gains in photon count rates and pile-up effects can be reduced through utilization of multiple detectors per pixel [14], multi-event TDCs [8], multi-channel TDCs per pixel [15], hybrid detectors [17] or by dead-time optimization [1], [18], [19], [20]. A further data bottleneck occurs however when the available readout I/O rate limits the practical data throughput rate [21], [22]. This prevents the full dynamic range of the SPADs from being utilized and slows the acquisition of the eventual time-stamp histograms on which downstream processing is based. This can be demonstrated more clearly with the following scenario. Assuming an 80 MHz laser source and a moderate 5% photon detection rate, 4 million-events/s can be captured per pixel which translates to 2.048 giga-events/s (or 22.528 Gbps with 11b/event) for a 512 pixel array. Again

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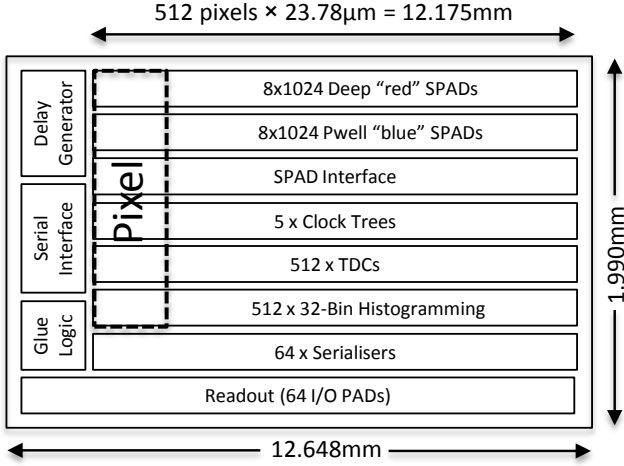


Fig. 1. Block diagram of the line sensor.

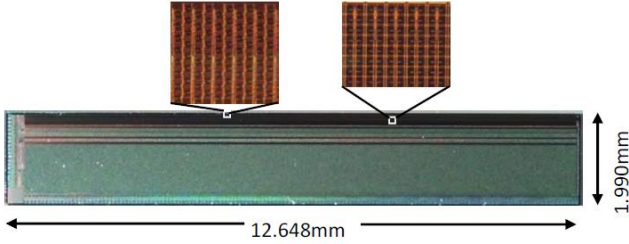


Fig. 2. Photomicrograph of the line sensor with inset showing blue and red SPADs of 5 pixels.

assuming an 80 MHz I/O data rate, such data throughput would require 282 parallel output pads to transfer the data off chip completely. As well as not being scalable, such an architecture would require a highly-parallel I/O that would significantly increase I/O power consumption and chip area, creating a severely pad-limited design. On the other hand, if the number of I/O pads are fixed to 64 (as an example), it would mean that 77.30% of the available photons would be lost due to the readout bottleneck.

In this paper, we address the above issues first by employing 16 SPADs per pixel and secondly by implementing on-chip histogramming for the first time at a *per-pixel* level achieving up to two orders of increase in SPAD photon processing rates. Photon events are directly recorded in the on-chip per-pixel histogram memory, enabling many more events to be captured for a given exposure time. This has two major benefits: reduced I/O power consumption (since only the final histograms are readout instead of reading out all photon events) and increased pixel dynamic range. Optical throughputs of 102.1 giga-events/s in single photon counting (SPC), 192.4 million-events/s in TCSPC and 16.5 giga-events/s in on-chip histogramming modes are achieved. Histogramming mode increases the photon count rate up to 85 times compared to TCSPC. This compares to throughputs of 8.5 giga-events/s in a 256×1 line sensor [9] and 900 million-events/s in a single point sensor [8] in state of the art TCSPC sensors.

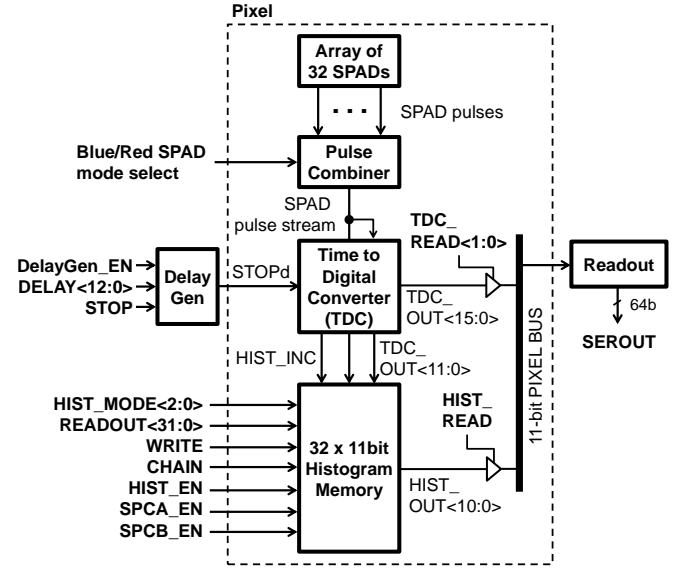


Fig. 3. Pixel block diagram.

The sensor is designed to enable high-throughput fluorescence lifetime imaging microscopy (FLIM) simultaneously in both time and spectral domains [23]. To allow contrast enhanced imaging of multiplexed fluorescent probes, fluorescence decays from multiple spectral regions can be adaptively selected and binned real-time in firmware. Furthermore a time-zooming capability in the design of the per-pixel histogramming TDC allows the sensor to adapt bin sizes to the fluorescent probes being used. Other applications of the sensor are in time-resolved spectroscopy such as the study of fluorescence transients [6], Förster resonance energy transfer (FRET) [24], and mixed fluorescence/Raman spectroscopy [3]. The wide zooming range and fine spectral bins of the sensor (with bin widths from 51.20 ps to 6.55 ns) allow long fluorescent decay times to be captured as well as short time scale Raman and narrow spectral features of time-resolved Raman signals. The sensor described in this paper was first presented in [25]. More details about the architecture implementation and an extended characterization are reported here.

The paper is organized as follows; Section II describes the top level design of the sensor, Section III focusses on the core of the TDC, Section IV describes the histogramming function, Section V introduces a novel delay generator block essential to the time-zooming functionality and Section VI briefly describes data readout. Sections VII and VIII provide electrical and optical characterization results culminating in a scanned multiplexed fluorescence lifetime image. Section IX concludes the paper.

II. LINE SENSOR DESIGN

A simplified block diagram of the sensor is shown in Fig. 1. The sensor has 2 SPAD line arrays, one optimized for the 450 nm to 550 nm wavelength range (blue SPADs), and the other optimized for 600 nm to 900 nm (red SPADs). Each pixel has a 2×8 array of blue and 2×8 array of red SPADs. The left and

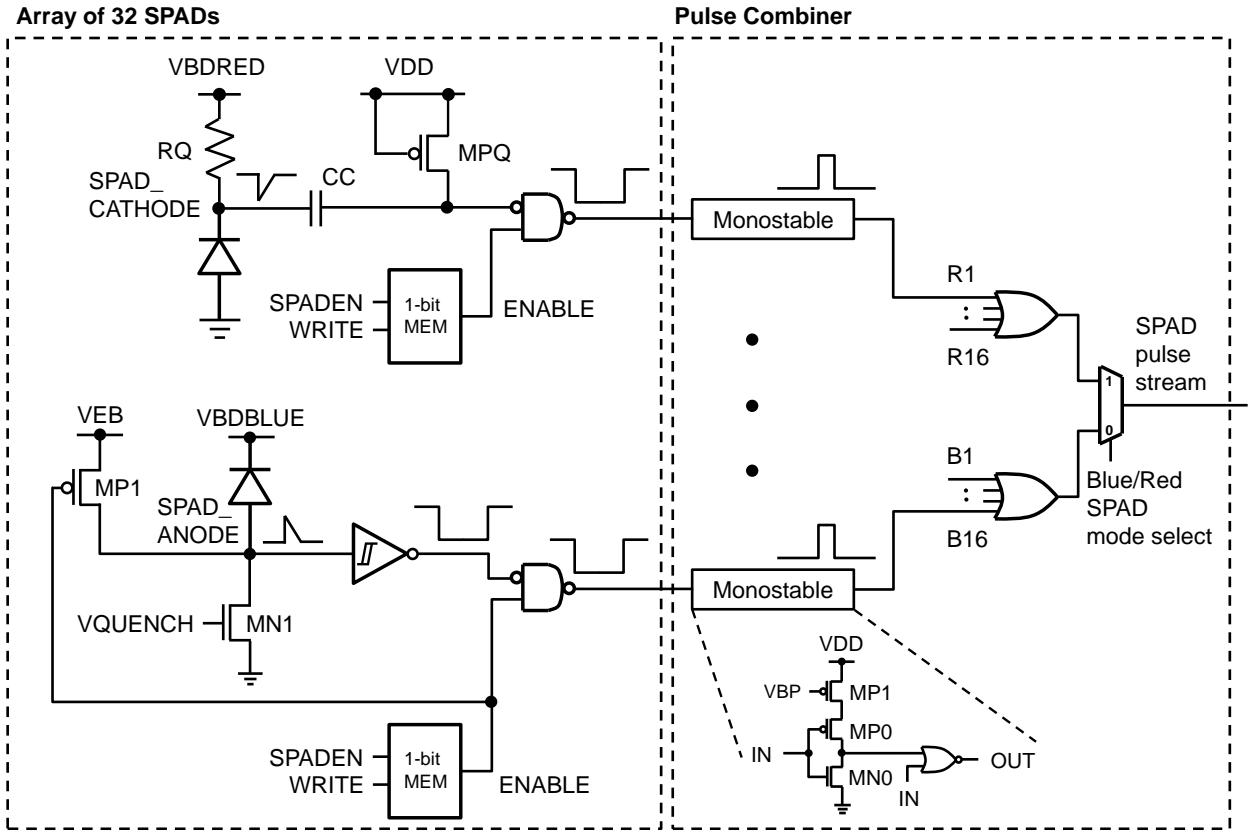


Fig. 4. Red and Blue SPAD front-end circuit schematic.

right SPADs can be read out separately to provide double the spatial resolution. In addition the sensor has 512×16 -bit, 51.20 ps TDCs; 512×32 -bin, 11-bit/bin histogram memory; $5 \times$ clock trees (one for distributing the laser synchronization signal to TDCs and the remaining 4 for generating two time-gates); a delay generator; a serial interface; $64 \times$ serialisers (i.e. one serialiser per 8 pixels); and a readout unit for managing reading out 512 pixels through 64 IO PADs. A photomicrograph of the line sensor is shown in Fig. 2. The die, measuring $12.648 \text{ mm} \times 1.990 \text{ mm}$, is fabricated in STMicroelectronics 130 nm CMOS imaging process. This process has been chosen since it provides industry-proven SPADs in a reasonable gate density [26]. In addition, this process, with its reduced height optical stack and anti-reflective coating, provides inherently good photon transmission, enhancing photon detection efficiency.

A block diagram of the pixel is shown in Fig. 3. Both blue and red SPADs have front-end logic that includes generation of digital pulses from SPAD events, quenching circuitry, and a single bit enable/disable memory cell for masking off high DCR SPADs for red SPADs and for both masking off as well as turning off high DCR SPADs for blue SPADs, as shown in Fig. 4. Sixteen red SPADs [27], employing a circular deep-n-well to p-substrate active region of $7.88 \mu\text{m}$ diameter, are arranged in an 8 rows by 2 columns format (with an array area of $23.78 \mu\text{m} \times 116.37 \mu\text{m}$) resulting in a 28.20% SPAD array fill-factor (FF). The red SPADs are interfaced to low voltage digital electronics via a $400 \text{ k}\Omega$ polysilicon resistor (RQ) and a 10 fF metal-oxide-

metal finger capacitor (CC). An off PMOS transistor MPQ maintains a high state through leakage current at the input of a NAND-gate allowing the SPAD output pulses to be masked by a serially programmed per-SPAD single bit memory cell. The red SPADs cannot easily be gated off because MOS transistors tolerant of high voltages at the SPAD cathode are not available.

Similar to red SPADs, sixteen blue SPADs [28], each employing a shallow p-well to deep-n-well active region, are arranged in an 8 rows by 2 columns format (with an array area of $23.78 \mu\text{m} \times 95.12 \mu\text{m}$). These SPADs are drawn as squares with rounded (super-ellipse) corners and have a diameter of $8.88 \mu\text{m}$. The deep-n-well cathode is shared between all blue SPADs to reduce spacing requirements, increasing the FF to 49.31%. As with the red SPADs, the blue SPAD outputs can be masked individually by a serially programmed per-SPAD single bit memory cell. Contrary to red SPADs, blue SPADs can be gated off or on by rapidly raising or lowering their anode by means of conventional low-voltage MOS transistors. As shown in Fig. 4, the SPAD cathode is connected to a common bias line (VBDBLUE) and the SPAD is turned off by pulling the SPAD anode to VEB ($\sim 3.3 \text{ V}$) via the PMOS and prevents the slow recharge of the SPAD from affecting the pulse combiner circuit.

The individual SPAD outputs are coupled to a pulse combiner circuit which acts as a compressor and combines the SPAD outputs into a single pulse stream, providing one short pulse per photon count. The relatively long SPAD pulses (tens of ns) are first compressed in time by per-SPAD monostable

devices providing a pulse shortening function to prevent overlapping pulses from obscuring each other, a technique termed temporal compression, as presented in [29]. The implemented monostables are current-starved and their current can be controlled through an external control voltage (VBP), hence allowing the width of their output pulses to be fine-tuned from 300 ps to 2.6 ns by varying VBP from 0 V to 0.7 V. The effect of monostables in photon count rates is studied in [30]. A second level of compression is implemented by ORing pulses from blue and red SPADs separately through OR trees (spatial compression), as shown in Fig. 4. Since only one SPAD variant can be enabled at a time, red or blue SPADs are selected through a serially programmed control signal, generating a pulse stream corresponding to the selected SPADs.

We used 32 SPADs (16 blue and 16 red) per pixel to increase sensitivity. Using multiple smaller SPADs per pixel also lowers jitter, crosstalk, and mean DCR as opposed to using a single larger equivalent SPAD [31]. In addition, high DCR SPADs can be eliminated, resulting in reducing the overall DCR leading to a more uniform DCR variation across the pixel array. The ellipsoid shape of the blue SPADs has been chosen to maximize FF whilst minimizing DCR [31]. Blue SPADs which are isolated from each other by an n-well, have been shown to have low crosstalk despite close proximity [32]. On the other hand Red SPADs share a resistive common substrate and exhibit significant electrical crosstalk at excess bias voltages beyond 1.5V. We have addressed this problem by choosing a circular layout style within a hexagonal matrix which maintains uniform anode separation. In addition, the red-SPAD area is chosen smaller at greater separation distance than blue SPADs (hence lower FF) in order to minimize charge flow during avalanche to reduce substrate-based electrical crosstalk.

As shown in Fig. 1, the SPADs are configured in a 16 rows by 2 columns array in each pixel. The top 8 rows being red SPADs and the bottom 8 rows being blue SPADs. The blue SPADs are connected to the front end circuitry in the SPAD interface block via 16 wires on 2 metal layers utilising the space between the two columns of SPADs in the pixel. A similar routing scheme is employed for the red SPADs, but this time using the space between the two columns of neighboring pixels SPADs. This routing scheme provides a layout that separates the blue and red SPADs routing into the space between alternating columns of SPADs. One implication of this routing scheme is that the wires for red SPADs routing are extended by 95.12 μm (i.e., the height of the blue SPAD rows) that has a negligible effect in overall SPAD timing performance.

III. TDC ARCHITECTURE

The TDC architecture is shown in Fig. 5. It supports both TCSPC and on-chip histogramming modes. The TDC is based on a gated ring oscillator (GRO) design reported in [28] which has a ~ 50 ps resolution and which was chosen for its small area footprint, making it suitable for long array implementations. The GRO has four pseudo-differential stages and it triggers a 13-bit ripple counter, providing the coarse output, while the 3-bit fine output is obtained by encoding its four internal nodes, resulting in a 16-bit TDC output. This allows targeting different classes of fluorescent molecules commonly used in lifetime imaging which have a wide range of fluorescence lifetimes. For

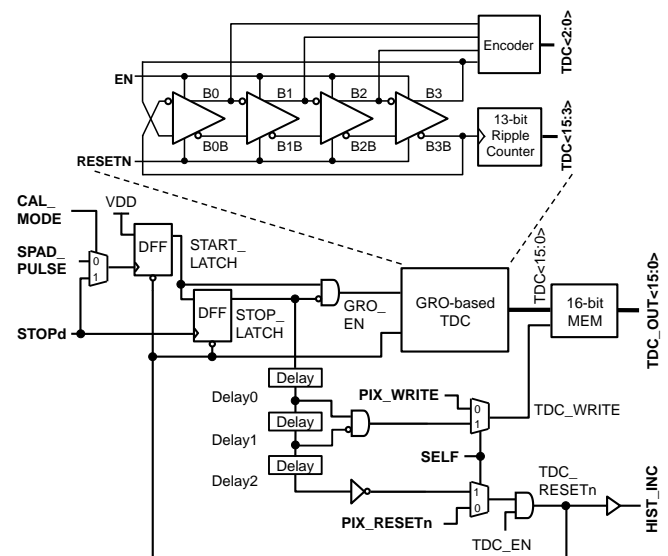


Fig. 5. Edge triggered self-resetting TDC block.

example, most organic dyes have lifetimes in the range of 1 – 20 ns (up to 90 ns); Quantum dots 10 – 30 ns (up to 500 ns); and Lanthanides from μ s (Yb, Nd) to ms (Eu, Tb) [33]. In order to minimize the TDC power consumption, the TDC is operated in reversed start-stop configuration [12] in which the GRO is started only when a SPAD pulse arrives from the SPAD array and stopped by a delayed version of the laser synchronization signal (STOPd). Secondly, the TDC is only enabled in TCSPC or on-chip histogramming modes through a serially programmed control signal (TDC_EN). Each TDC of the pixel array can be compensated for process, voltage and temperature (PVT) variations by calibrating its power supply voltage using a 5-bit resistor ladder DAC (not shown in Fig. 5) which allows fine tuning each TDC power supply voltage between two bias supply voltages distributed to all TDCs. When put to the calibration mode by asserting the CAL_MODE signal high, each TDC measures the STOPd period and the results are used to fine tune each TDC power supply voltage by a serially programmed 5-bit code. This is repeated periodically to keep all TDCs PVT compensated.

In TCSPC mode, TDC_WRITE and TDC_RESETn control signals for all TDCs are provided by the global PIX_WRITE and PIX_RESETn control signals for storing generated time-event values to local 16-bit memory units before being read-out via a shared 11-bit pixel bus and resetting the TDCs for the next exposure cycle. Global PIX_WRITE and PIX_RESETn signals are generated externally (by an FPGA) and distributed to all pixels. The time elapsed between two PIX_RESETn pulses define the exposure time which is normally tens or hundreds times longer than the laser pulse period since the expected photon count rate is $<10\%$ of the laser period in order to avoid pile-up issues. In TCSPC mode a maximum of one photon per exposure cycle can be captured since there is only one TDC per pixel and only the first photon can be captured. TDCs cannot process additional photons before their current data is readout off-chip and they are reset globally at the end of an exposure cycle. Fig. 6(a) shows a sample timing diagram for operating the TDC in TCSPC mode.

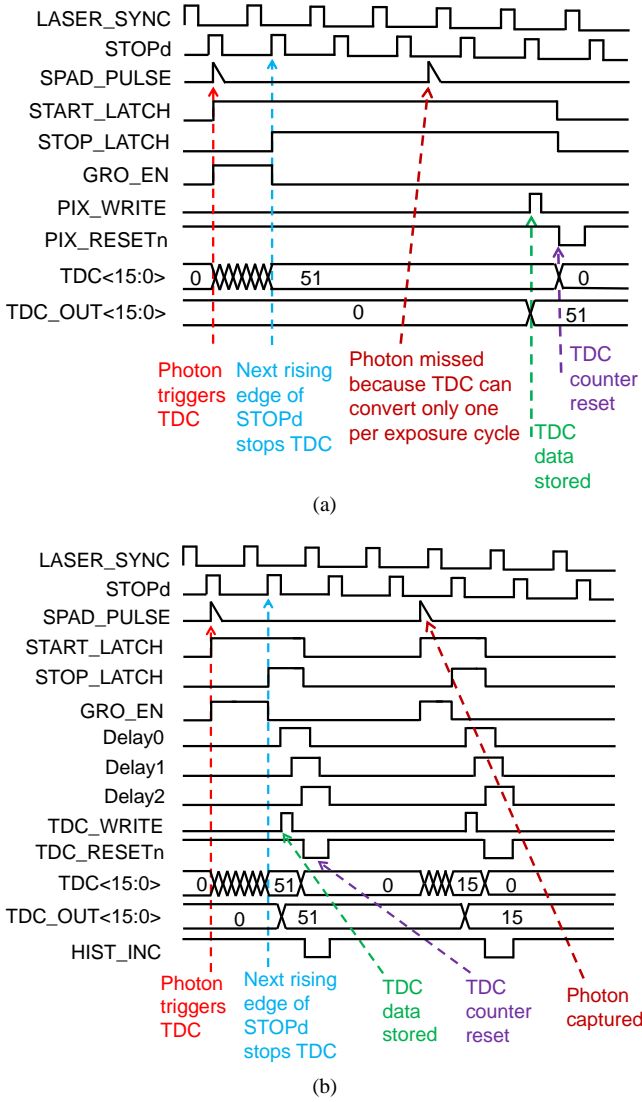


Fig. 6. TDC timing diagram: (a) TCSPC mode (SELF = 0), (b) Histogram mode (SELF = 1).

In on-chip histogramming mode, TDC_WRITE and TDC_RESETh control signals are generated automatically on-chip and independently for each pixel (using delayed versions of the STOP_LATCH signal) by selecting the self-resetting mode through a serially programmed control signal (SELF), as shown in Fig. 5. This enables multiple photons (up to one photon per laser period) to be captured and converted to time events per exposure cycle. This is one of the key advantages of the sensor presented. The maximum number of photons which can be captured in this mode is one photon per laser period since there is only one TDC per pixel and TDC_WRITE and TDC_RESETh signals are generated from the STOP_LATCH signal which is in turn derived from the STOPd signal (a delayed version of the LASER_SYNC signal), as shown in Fig. 5 and Fig. 6(b). A triggering signal (HIST_INC) is generated from the TDC_RESETh signal to increment the selected counter in the histogramming block. The reason for generating the HIST_INC from TDC_RESETh is to allow enough time for the Histogram Decoder block to select the histogram counter to increment based on the current TDC output and the selected histogram mode (explained in more detail below in Section IV).

Fig. 6(b) shows a sample timing diagram of the TDC operation in histogram mode.

IV. HISTOGRAM ARCHITECTURE

The histogram block has 32 bins with 11-bits/bin where the msb is used as an overflow flag. For increased dynamic range every two consecutive bin pairs can be chained together, halving the number of bins to 16 while increasing the bin depth to 21-bits, including one overflow bit. In addition, each bin width in time can be configured from 51.2 ps to 6.55 ns under the control of the HIST_MODE parameter, providing a histogram window range from 1.64 ns to 209.92 ns. For example, when HIST_MODE is set to 0, each bin corresponds to 51.2 ps, which is the minimum and determined by the TDC resolution, providing a histogram window ranging from 0 to 1.64 ns. Similarly, when HIST_MODE is set to 1, each bin corresponds to 102.4 ps, and the histogram window range is hence extended to 3.28 ns, and so on. In chain mode, the histogram window range remain the same while both the bin depth and bin width in time double. When used together with a delay generator (external or on-chip), this feature (i.e. changing bin width) allows positioning of the histogram window and zooming to the peak of the fluorescence lifetime decay of a fluorescent sample. It is also worth noting that although the TDC can generate up to 16-bit timestamps, the histogram block utilizes only up to the first 12-bits of the TDC output since this provides more than enough range (i.e. up to 209.6 ns) for most Raman and fluorescence lifetime applications.

Fig. 7 shows the top level histogram block diagram which comprises the “Histogram Decoder” and “Histogram Memory” blocks. When the histogram mode is enabled by the HIST_EN signal, the role of the Histogram Decoder block is first to validate the current TDC data (i.e. timestamp) to make sure that it is within the histogram window range which is set by the HIST_MODE parameter. The validation process is performed by checking higher bits of TDC_OUT which are outside of the selected histogram window range. For example, if HIST_MODE is set to 0, bits 5 to 11 are checked. If HIST_MODE is set to 1, bits 6 to 11 are checked, and so on. If any of these bits are HIGH, the current timestamp is regarded as invalid and discarded by setting TDC_VAL to 0 (by setting the VALID signal to 0), as shown in the bottom inset of Fig. 8. Otherwise, it is passed to the next block which controls the histogram window range by selecting the appropriate chunks of 5-bits of TDC_VAL based on the HIST_MODE parameter. For example, if HIST_MODE is set to 0, the first 5-bits of TDC_VAL are selected (i.e. TDC_VAL<4:0>), resulting in setting each histogram bin width to 51.2 ps (i.e. one timestamp per bin), and hence realizing a histogram window from 0 to 1.64 ns. Similarly, if HIST_MODE is set to 1, bits 1 to 5 are selected (i.e. TDC_VAL<5:1>), resulting in setting each histogram bin width to 102.4 ps (i.e. two timestamps per bin), and hence realizing a histogram window from 0 to 3.28 ns, and so on. The selection of 5-bit chunks of TDC_VAL is implemented by using 5 8-to-1 multiplexers (one multiplexer per bit), as shown in the top inset of Fig. 8. The selected 5-bit chunks of TDC_VAL are then passed to a 5 to 32 decoder block which generates enable signals for selecting 1 out of 32 bins (i.e. ripple counters) to be incremented. The Histogram Decoder is also

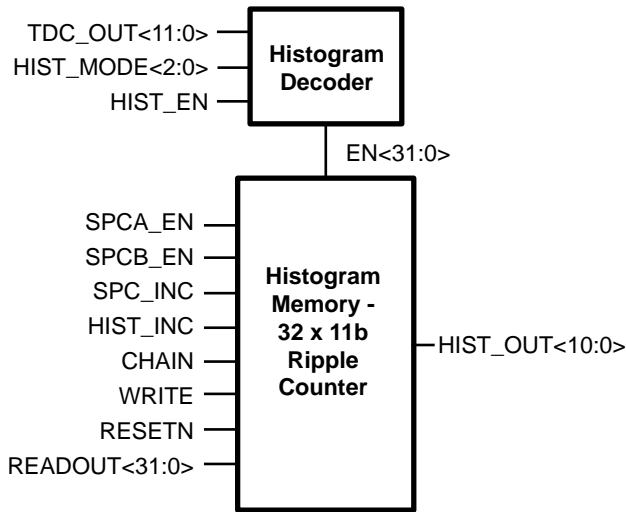


Fig. 7. Top level histogram block diagram.

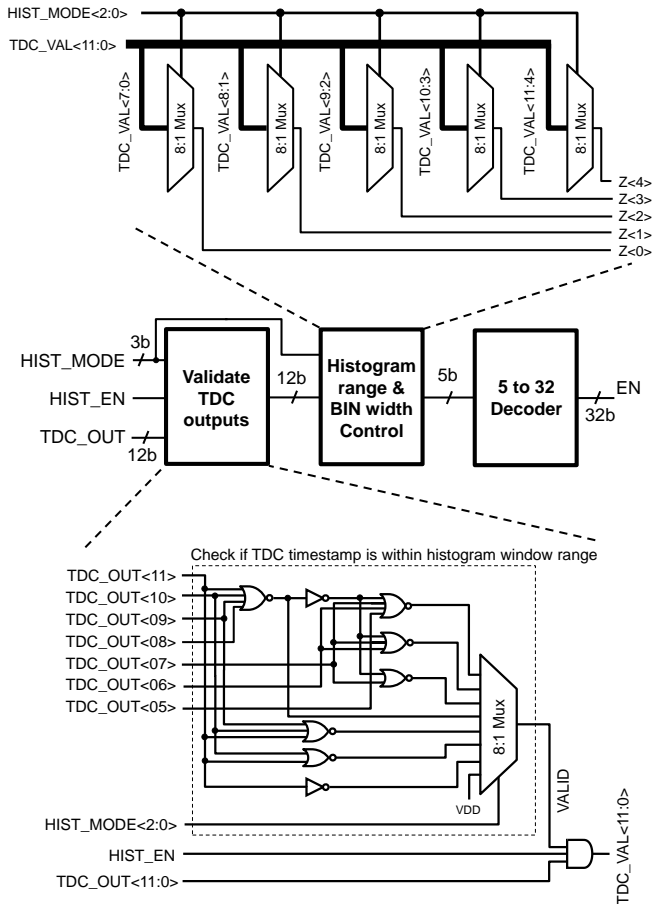


Fig. 8. Histogram decoder block diagram.

responsible for detecting 0 TDC_VAL cases (not shown in Fig. 8) which need to be excluded from building a histogram of timestamps since they do not represent any valuable information other than indicating that they were outside of the set histogram window range.

Fig. 9 shows a block diagram of the Histogram Memory which consists of 32 bins. Each bin is implemented as 11-bit ripple counters. In addition, each bin has mux-based memory

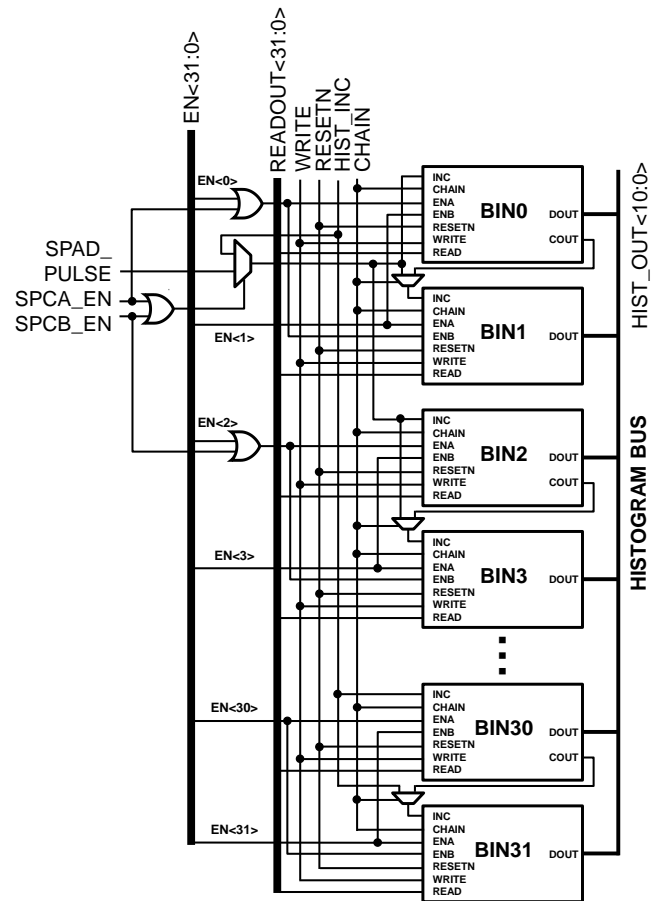


Fig. 9. Histogram memory block diagram.

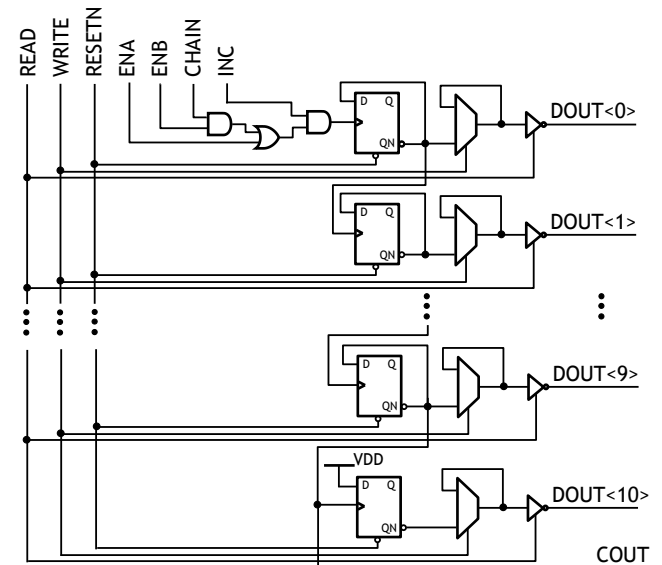


Fig. 10. Histogram bin block diagram.

units for saving final counter contents, and tri-state buffers for connecting the bin to the histogram bus. A block diagram of the bin is shown in Fig. 10. As stated before, for increased dynamic range every two consecutive bin pairs can be chained together. This is done by setting CHAIN (a serially programmed register)

to HIGH, which connects COUT (i.e. bit DOUT<9>) of one bin to the INC input of the next bin via a mux. The msb (i.e. DOUT<10>) of each bin is used as an overflow flag. For every timestamped photon, indicated by the HIST_INC signal which is generated by the TDC block, one bin (or bin pair in CHAIN mode) which is enabled by EN<31:0> (generated by the Histogram Decoder block as described above) is incremented. At the end of an exposure cycle, the contents of each ripple counter are saved to mux-based memory units by asserting WRITE signal HIGH, and counters are reset (by RESETN) for the next exposure cycle. This allows a new exposure cycle to be initiated while the data of the previous exposure cycle is being read out. Each bin is read out in sequence (under the control of READOUT<31:0>) through a tri-stated 11-bit histogram bus which is subsequently connected to the 11-bit pixel bus.

A portion of the Histogram Memory block is shared between histogram and SPC modes. In SPC mode, enabled by either SPCA_EN or SPCB_EN control signals, the first 4 histogram bins are used to create one or two independent time-gated 20-bit counters (SPCA and/or SPCB), allowing for rapid fluorescence lifetime estimations when both counters are enabled or just capturing intensity mode data with only one of the counters enabled. As in histogram mode, both counters can be operated in chain mode for increased dynamic range. The time-gated SPC feature is not discussed further in this paper. In SPC mode, the enabled counters are triggered directly by SPAD pulses coming from the Pulse Combiner block, by by-passing the TDC.

V. DELAY GENERATOR

Fig. 11 shows the block diagram of the on-chip delay generator, used for positioning the histogram window such that it covers the target fluorescence decay by delaying the laser sync (i.e. STOP) signal by an appropriate amount. As an alternative to a commonly used delay line approach [34], the delay generator was implemented based on the same GRO used for TDCs in order to increase the delay range without increasing the circuit area of the delay generator too much. As described in Section III, the GRO has 8 phases and having ~63 ps delay between phases leads to 504 ps delay per loop. Therefore, for a given delay, first the required GRO phase and the number of loops are determined. This is simply done by selecting the first 3-bits of a delay code (i.e. DELAY<2:0>) for determining the required GRO phase, and the remaining bits (i.e. DELAY<12:3>) provide the required number of loops plus one. Therefore, using a 13-bit delay code provides delays up to ~516 ns in steps of ~63 ps. The required GRO phase is selected with an 8-to-1 mux which is then used to trigger a 10-bit ripple down counter which is initially loaded with the required number of loops. A zero crossing detection circuit monitors the counter output and once the zero crossing is detected the delay generator output is raised HIGH by using a D-type flip-flop (DFF) which represents the delayed rising edge of the STOP signal (i.e. STOPd). Then the delay generator is self-reset and the counter is re-loaded for the next cycle. The self-resetting is realized by generating an internal reset signal RESETN_INT (separate from the system reset SYSRESETN) by using delayed versions of STOPd. The loading of the counter is performed in two steps. In the first step, all counter bits are set to HIGH by RESETN

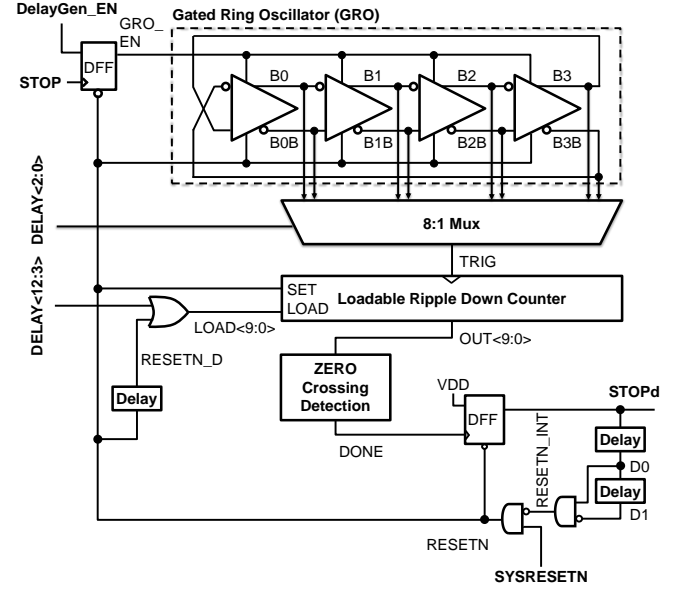


Fig. 11. GRO-based delay generator block diagram.

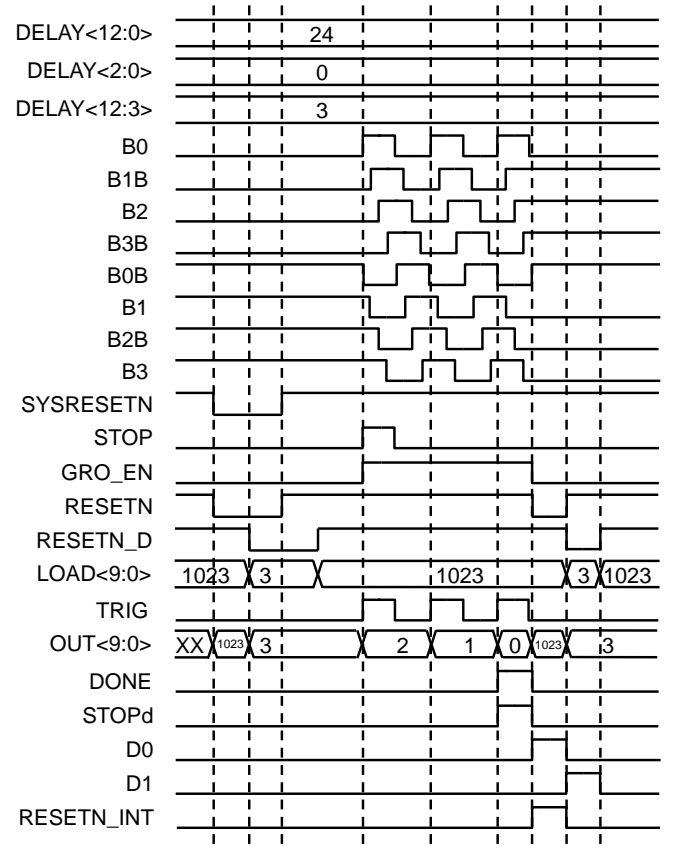


Fig. 12. Delay generator timing diagram.

signal. In the second step, the counter bits selected by DELAY<12:3> are set to LOW by using a delayed version of the RESETN signal. Fig. 12 shows a sample timing diagram for realizing a delay of 1008 ps as an example.

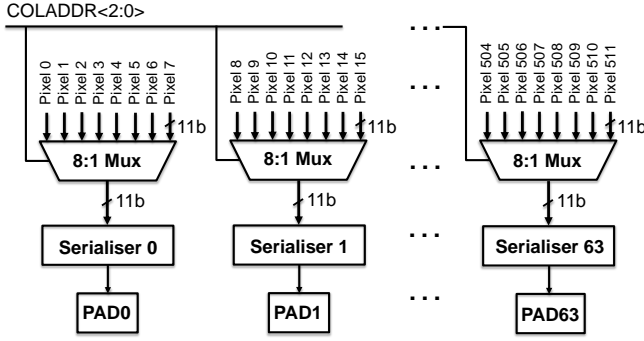


Fig. 13. Readout block diagram.

VI. READOUT

The readout of the 512 pixel array is performed through 64 serializer units, each feeding to an I/O pad. Each serializer unit, therefore, is shared by 8 pixels, as shown in Fig. 13. With a 40-MHz system clock, this results in a full chip readout time of 2.2 μ s, corresponding to 454 thousand spectra/s in SPC (unchained) and TCSPC modes, 227 thousand spectra/s in chained SPC mode, and 14.2 thousand spectra/s in histogram mode.

VII. MEASUREMENT RESULTS

A. Dark Count Rate (DCR)

The DCR was measured at room temperature for different excess bias voltages for both blue and red SPADs, as shown in Fig. 14. DCR measurements were performed by enabling one SPAD per pixel at a time and operating the sensor in SPC mode. For blue SPADs, the measured breakdown voltage was 14.1 V and the median DCR was 76 counts per second (cps) at 1 V excess bias voltage which increased exponentially with the applied voltage. While red SPADs had a higher breakdown voltage of 24.6 V, they had much lower median DCR of only 12 cps at 1 V excess bias voltage which also increased exponentially with the applied voltage.

B. Photon Detection Efficiency (PDE)

The SPAD PDE was measured to characterize the sensitivity of the pixels at different wavelengths. Fig. 15 shows the PDE versus wavelength, measured at 1 V excess bias voltage by sweeping the excitation light wavelength from 350 nm to 1050 nm in steps of 10 nm for both blue and red SPADs, enabling one SPAD per pixel at a time. The data from all pixels was then averaged. For blue SPADs, the peak PDE is 17% at 480 nm, while for red SPADs, the peak PDE is 7% at 620 nm. The results also show that while blue SPADs provide up to ~15% higher PDE for wavelengths below 550 nm, for higher wavelengths red SPADs provide up to two times higher PDE, as expected.

C. TDC linearity

The optical statistical code density test [35] was performed using SPAD dark counts to estimate the TDC linearity. The results are shown in Fig. 16. The average resolution is 51.20 ps, with less than 1 ps of standard deviation (i.e. 0.68 ps) between all TDCs of the pixel array without applying any calibration.

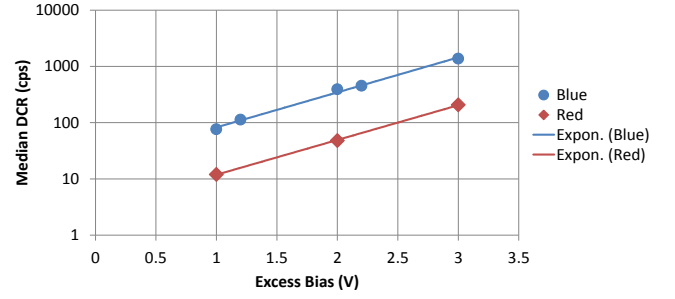


Fig. 14. Median DCR versus excess bias voltage of blue and red SPADs.

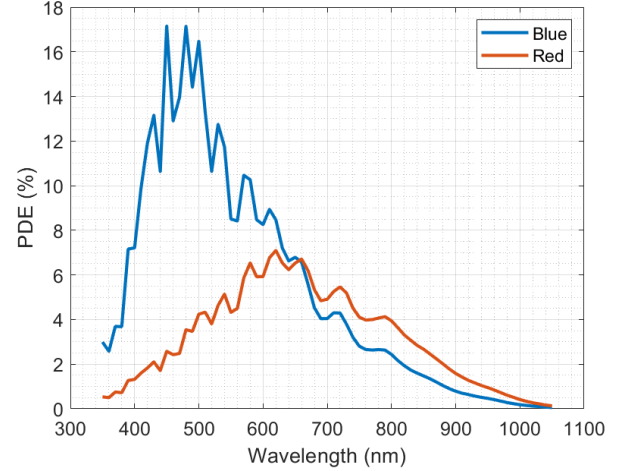


Fig. 15. PDE versus wavelength, measured in 10nm steps and at 1V excess bias voltage for both blue and red SPADs. Data has been averaged over all 512 pixels.

The timing skew across the pixel array is 3 TDC codes (i.e. ~154 ps), as shown in Fig. 16(b). The differential and integral nonlinearity (DNL/INL) performance of a typical TDC (in this case Pixel 100 was chosen) in a 50 ns range is shown in Figs. 16(c) and 16(d) respectively. The worst-case measured DNL is +0.37/-0.37 LSB and INL is +3.10/-3.96 LSB. We estimate that this non-linearity can lead to up to 1% error in the estimated lifetimes which is not significant. The effect for shorter lifetimes (< 4 ns) will be even less since the max/min INL is only +1.24/-0.69 for the first 300 codes. Furthermore, both DNL and INL can be corrected off-chip by applying some correction algorithms [36]. It is also worth noting that small DNL/INL effects can be neglected for applications (as in our application) where relative lifetimes are more important than absolute values.

D. Instrument Response Function (IRF)

The instrument response function (IRF) was recorded for wavelengths from 475 nm to 900 nm in steps of 25 nm at 1 V excess bias voltage and enabling a single SPAD per pixel. For this a supercontinuum laser (WhiteLase micro, Fianium Ltd., UK) was filtered for the desired wavelength with a tunable filter (Laser Line tunable Filter, Fianium Ltd., UK) providing 2.5 nm bandwidth. The free-space collimated beam of the filter output was attenuated by a neutral density filter to avoid photon pile-up and diffused to cover the whole sensor array. For each wavelength, 100K samples were captured in TCSPC mode with

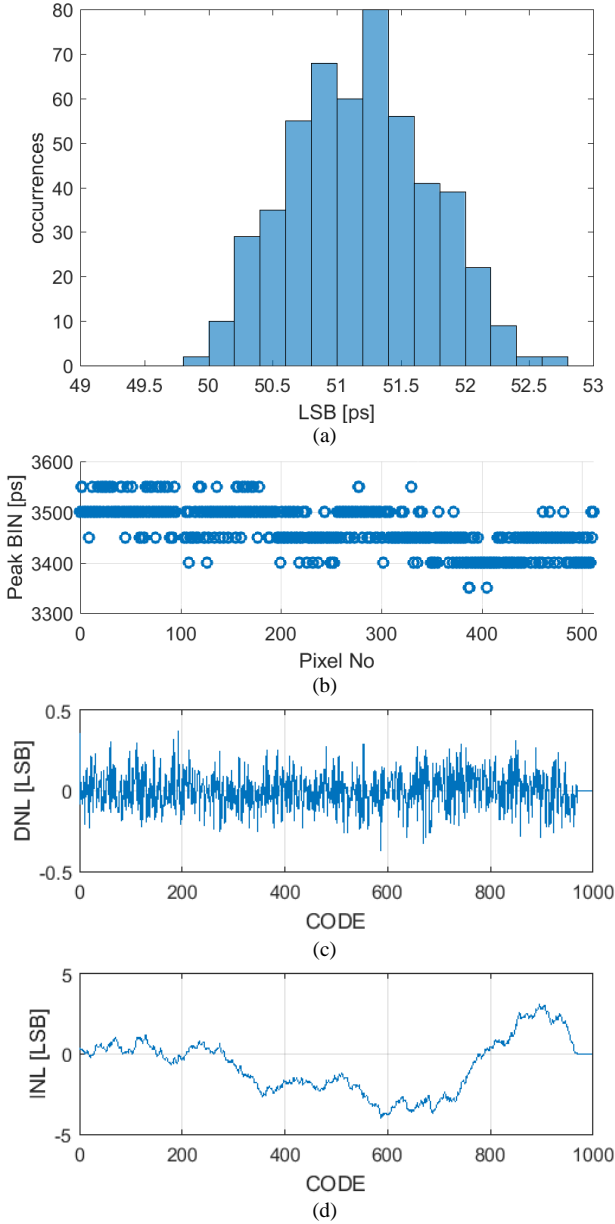


Fig. 16. Uncalibrated TDC characterization results. (a) LSB uniformity (mean = 51.20 ps, std = 0.68 ps), (b) Timing skews of the TDCs across the pixel array, (c) DNL max/min: +0.37LSB/-0.37LSB, (d) INL max/min: +3.10LSB/-3.96LSB. DNL and INL results are for pixel 100 which represents a typical TDC.

an exposure time of 10 μ s per sample. This was followed by generating a histogram of timestamps per pixel, where each bin corresponds to 51.20 ps which is determined by the TDC resolution. A Gaussian curve fitting function was then applied to estimate the full width at half maximum (FWHM) IRF of each pixel. Fig. 17(a) shows IRFs of typical blue and red SPADs. The IRF of the red SPADs has a longer exponential tail, also known as a ‘diffusion tail’ due to the wide photo-carrier diffusion region for enhanced collection of longer wavelength photons [27]. Fig. 17(b) shows FWHM IRFs of blue SPADs @500 nm (mean FWHM = 162 ps) and red SPADs @700 nm (mean FWHM = 127 ps). Fig. 17(c) shows the mean FWHM IRFs of blue and red SPADs versus wavelength. Clearly, blue SPADs exhibit lower FWHM IRFs and variation

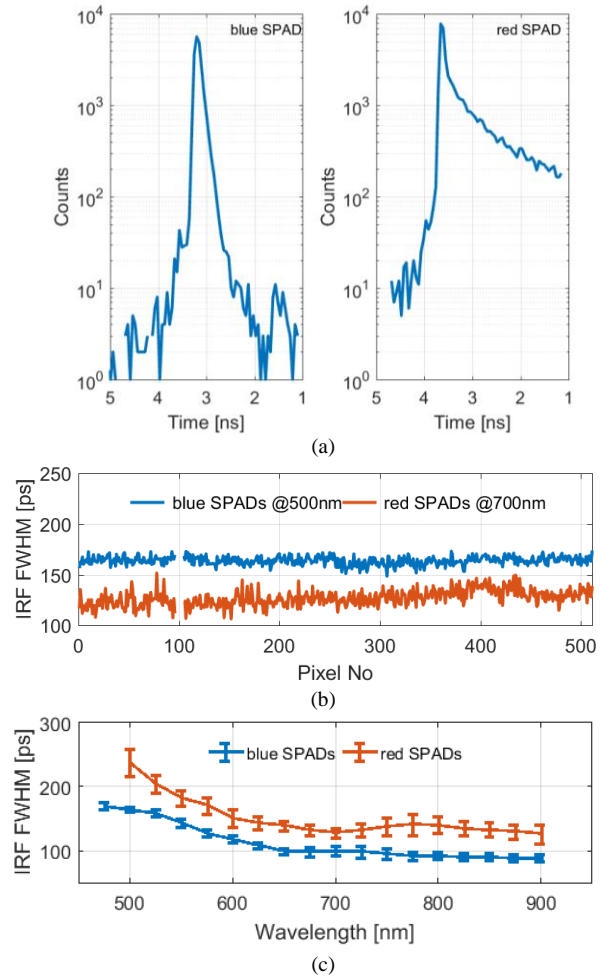


Fig. 17. IRF measurements with 1V excess bias voltage. (a) IRFs of typical blue and red SPADs, (b) FWHM IRFs of blue SPADs @500nm (Mean FWHM = 162 ps) and red SPADs @700nm (mean FWHM = 127 ps), (c) Mean FWHM IRFs of blue and red SPADs versus wavelength.

across the wavelength range compared to red SPADs and in general IRFs of both blue and red SPADs improve with increased wavelength. Having such narrow FWHM IRFs means that the IRF will have negligible effect on the fluorescence lifetime estimations for lifetimes > 1 ns. The IRF will need to be taken into account (by applying deconvolution to fluorescence decays) for very short lifetimes which do not apply to most FLIM applications. Furthermore, in some applications, similar to DNL/INL effects, small IRF effects in the accuracy of estimated lifetimes can be neglected. For instance, in our application we are mostly interested in relative lifetime comparisons (for distinguishing different fluorophores) instead of absolute values.

E. Delay Generator Characterization

The delay generator was characterized by delaying a 20 MHz laser synchronization signal up to 50 ns by sweeping the delay code from 0 to 800 in steps of one delay code at a time and repeating the test for at least 5000 times per delay code. Fig 18(a) shows the mean generated delay vs delay code, together with a linearly fitted delay line with a mean delay of 62.81 ps per delay code. The error, estimated as the difference between

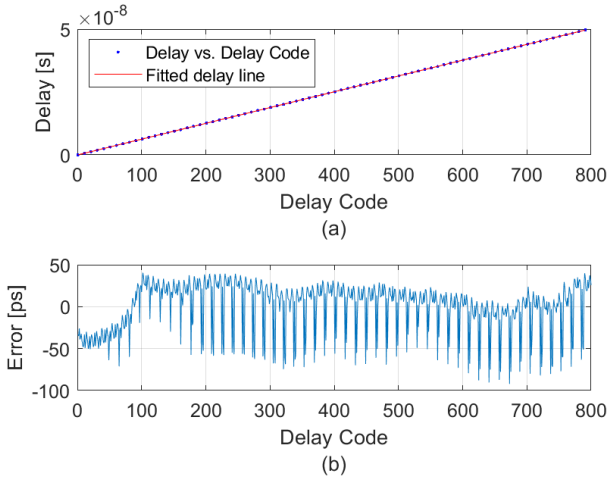


Fig. 18. Delay generator characterization results. (a) Mean generated delay vs delay code over a 50 ns delay range. A linearly fitted delay line is also shown. Generated delays are shown for every 10 delay codes in order to leave space for the fitted delay line. (b) Error in generated delays over the same 50 ns delay range, where the error is estimated as the difference between the measured and expected delays per delay code.

the measured and expected delays, per delay code is also shown in Fig 18(b), varying between $\pm 50/100$ ps over the whole 50 ns delay range.

VIII. OPTICAL PERFORMANCE

The optical performance of the sensor has been evaluated using only the blue SPADs which are best suited to organic fluorophores emitting at visible wavelengths < 700 nm.

A. Count rate

In order to evaluate the maximal optical performance of the line sensor, blue SPADs were illuminated with a current controlled LED, operated in continuous wave mode for SPC and in trigger mode (at 100 MHz) for TCSPC and histogram mode measurements. Optical throughputs of 102.1 giga-events/s in SPC mode, 192.4 million-events/s in TCSPC mode and 16.5 giga-events/s in histogram mode were achieved with $VEB = 1$ V and $VQUENCH = 2$ V. This corresponds to detecting up to 85 times more events in histogram mode compared to TCSPC mode. The results also show that in histogram mode on average one event in every 31 ns is detected per pixel, corresponding to one event for every 3 triggers, approaching the maximum one event per trigger limit. Fig. 19 shows the counts per pixel in SPC, TCSPC, and histogram modes, including the median DCR for comparisons.

B. Spectrally Resolved FLIM

In order to capture spectrally resolved fluorescence lifetime data, dispersive optics are required to separate the light spectrally onto the sensor. The optical setup is shown in Fig. 20. A separate epifluorescence configuration is used to excite and then collect the fluorescence from the sample. Light is collected from the sample via beam scanning optics, similar to a conventional confocal microscope, before being passed to the spectrometer system. The fluorescence is relayed by a multimode fiber to the spectrograph consisting of dispersive optics with the line sensor placed in focus, again in a

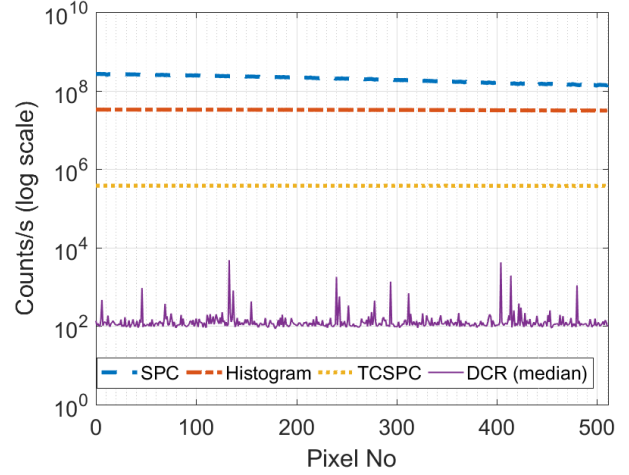


Fig. 19. Maximal count rate comparisons for blue SPADs (with $VEB = 1$ V & $VQUENCH = 2$ V).

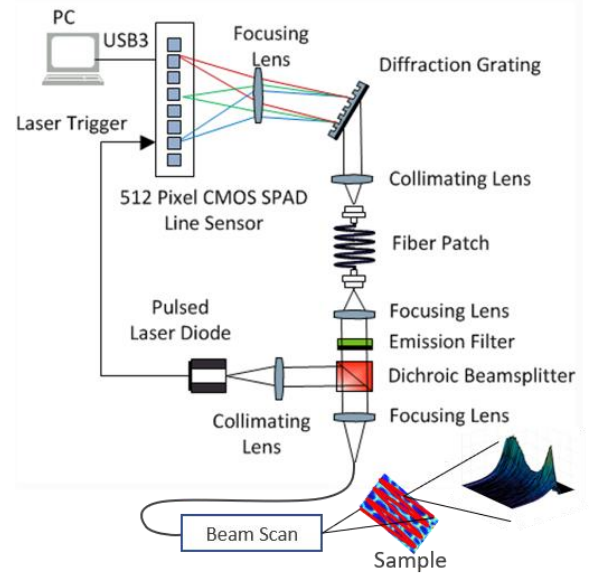


Fig. 20. Optical setup.

configuration used in most confocal microscopes. The image is thus built up pixel by pixel with the sensor producing time resolved spectra for each sampling point. In the experiments, the sample was illuminated by a Hamamatsu PLP10 483 nm pulsed laser diode at 20 MHz repetition rate. Peak power of the 483 nm pulsed laser was 349 mW, and the pulse length was 60 ps. Spectrograph diffraction was accomplished using a volume phase holographic grating (600 lp/mm at 600 nm) with collimating and focusing lens optimized for efficiency and spectral resolution. To cover the 135 nm wavelength span across the 512 pixels of the line sensor the collimating lens used was a 50 mm focal length achromat, while the focusing lens was a 75 mm focal length achromat.

In order to demonstrate the time-resolving spectral and imaging capabilities of the sensor we investigated fluorescent lifetimes of a Fluorescein and Rhodamine mixture and a specially prepared imaging test sample, having ~ 10 μm silica microspheres with Fluorescein, NBD, Rhodamine and Cy5 covalently attached. Fluorescein and NBD are green dyes with

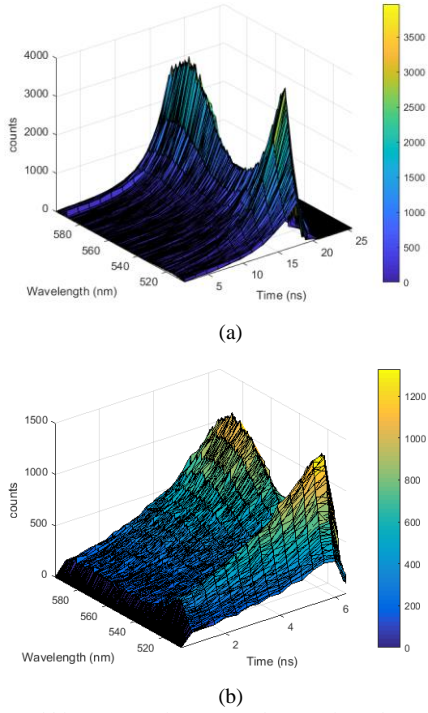


Fig. 21. Spectral histograms of a 10 μM Fluorescein and 100 μM Rhodamine mixture captured in histogram mode with 10 ms exposure time and (a) 1.64 ns/bin (i.e. HIST_MODE = 4 & CHAIN = 1) and (b) 409.6 ps/bin (i.e. HIST_MODE = 2 & CHAIN = 1) modes.

a lifetime of 4 ns and 2.5 ns respectively, whereas Rhodamine and Cy5 are red dyes with a lifetime of 1.5 ns and 1 ns respectively.

Fig. 21(a) shows time-resolved spectra of a 10 μM Fluorescein and 100 μM Rhodamine mixture captured in histogram mode with a 10 ms exposure time and 1.64 ns bin width (i.e. HIST_MODE = 4 & CHAIN = 1). The peak at 527 nm wavelength is due to the Fluorescein dye and has a longer lifetime compared to the Rhodamine dye which peaks at 584 nm. In order to demonstrate the zooming feature of the histogram mode, another time-resolved spectrum was captured by narrowing the bin width down to 409.6 ps and keeping the histogram window positioned around the histogram peaks by delaying the laser sync signal by an appropriate amount. It is worth noting that by narrowing the bin width, peak counts get reduced for the same exposure time, as shown in Fig. 21(b). This is expected since each bin gets fewer time-stamps from the TDCs. It is also clear that by narrowing the bin width the full decays of fluorophores with longer lifetimes are truncated. Therefore, the bin width must be typically selected to cover the range of expected decay times of the fluorophores under investigation. These experiments were performed without utilizing the beam scanning part of the optical setup shown in Fig. 20, since the sample used was very uniform.

Spectral lifetime imaging experiments were carried out with the specially prepared multi-fluorophore imaging test sample described above. For these experiments, the highest 4 DCR SPADs per pixel were turned off in order to reduce the overall pixel DCR. To test the sensor's capability to use fluorescence lifetime to distinguish between fluorophores we chose three

spectral bands for time-resolved lifetime investigations: Band I (500 nm – 544 nm), Band II (550 nm – 600 nm) and Band III (600 nm – 635 nm). These bands are fully programmable and implemented in firmware for higher performance (compared to a software based implementation). An exposure time of 85 μs per scan was applied, resulting in 8.7 seconds per 320×320 image frame. It is worth mentioning that in SPC mode the frame rate can be increased by reducing the exposure time. However, the same does not apply to histogram mode since the whole histogram data (i.e. 32 bins/pixel) needs to be readout at the end of each exposure cycle, resulting in longer time intervals between exposure cycles. The minimum exposure time for SPC and histogram modes can be determined by the following equation:

$$\#bins_per_pixel * 11bits_per_bin * 8 * clock_period \quad (1)$$

where the number of bins is 1 (unchained) or 2 (chained) in SPC and 32 (both chained and unchained) in histogram modes, as described in Section IV. Therefore, the options for increasing the frame rate in histogram mode include increasing the system clock frequency, reducing the number of histogram bins, or reducing the frame size.

For each pixel of a 320×320 scanned image, three sets of histograms (one per wavelength band) were obtained in unchained mode with bin width set to 819.2 ps (i.e. HIST_MODE = 4 & CHAIN = 0). Fluorescence lifetimes were estimated from these histograms by applying the Centre-of-Mass Method (CMM) [37]. The intensity and lifetime results for all three bands are shown in Fig. 22. Clearly all fluorophores look very similar in intensity mode images, as shown in Figs. 22(a-c), and therefore it is hard to separate them by intensity alone. In time-resolved mode, however, different fluorophores become more visible and easier to distinguish from each other based on their measured lifetimes, as shown in Figs. 22(d-f). For each band, lifetimes from all pixels are collected into histograms in Figs. 22(g-i). It is clear that two dyes (Fluorescein and NBD) appear in Band 1, as supported by the two lifetime histogram peaks around 2.5 ns and 4 ns, as shown in Fig. 22(g). Bands 2 and 3 show a third peak around 1.5 ns in their lifetime histograms, as shown in Figs. 22(h-i), which corresponds to Rhodamine. It is also noticeable that the presence of Fluorescein diminishes significantly in Band 3. This is expected since Fluorescein emission peaks at ~ 520 nm and hence only a small part of its spectral emission tail is detected in Band 3. NBD has a strong presence in all 3 bands since its emission peaks at ~ 530 nm and it has a very broad spectral emission. The fourth dye (Cy5) is not present in any of the bands since it was not excited by the blue laser used and its emission sits out-with the spectral range dispersed onto the sensor.

As the maximum signal-to-noise ratio (SNR) of fluorescence lifetimes can be estimated by \sqrt{N} , where N is the number of recorded photons [12], [38], we have the following maximum SNRs for lifetimes in Fig. 21(d-f): 162 (Band 1), 172 (Band 2), and 82 (Band 3) with a min SNR of 28 set for all bands. These SNRs correspond to relative standard deviations of 0.62% – 3.57%, 0.58% – 3.57%, and 1.22% – 3.57% for Bands 1-3

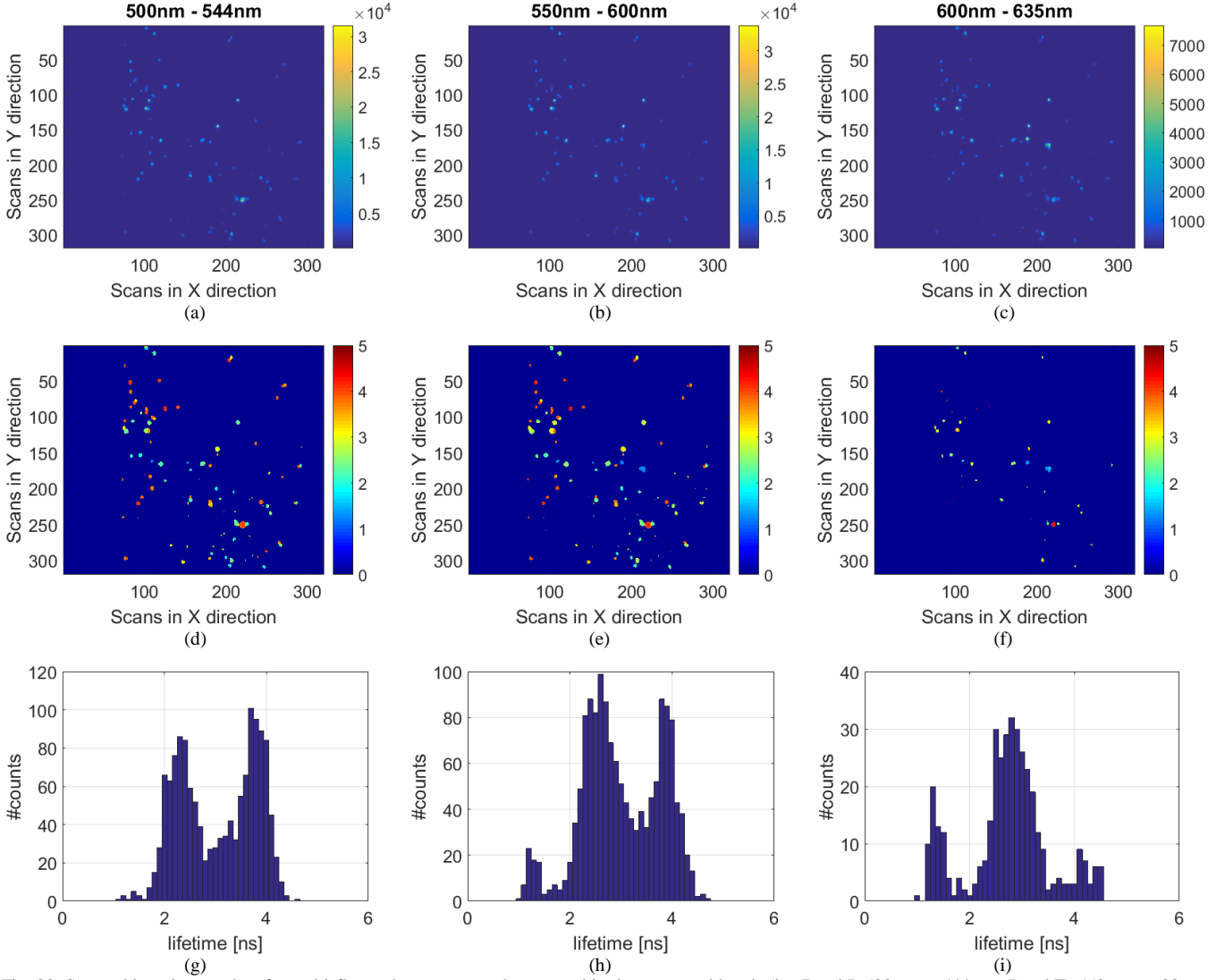


Fig. 22. Spectral imaging results of a multi-fluorophore test sample captured in three spectral bands (i.e. Band I: 500 nm – 544 nm, Band II: 550 nm - 600 nm and Band III: 600 nm - 635 nm) in unchained histogram mode with 85 μ s exposure time per image pixel and 819.2ps/bin (i.e. HIST_MODE = 4 & CHAIN = 0). (a)-(c) Number of photon counts in intensity mode, (d)-(f) Lifetime (ns), (g)-(i) Lifetime histograms.

respectively, where the relative standard deviation is given by $1/SNR$ [12], [38].

Table I summarizes the performance of the line sensor, whereas Table II provides comparisons with state-of-the-art line sensors.

IX. CONCLUSION

We have demonstrated a 16.5 giga-events per second CMOS SPAD line sensor which promises to enhance time-resolved spectroscopy and imaging applications and enable new ones. We have presented the first implementation of an innovative per-pixel on-chip histogram architecture. The histogram architecture combines delay offsetting and histogram bin size adjustment which allows optimal fitting of fluorescence decays into the available histogram bins. While previous CMOS SPAD architectures parallelized single photon detection by adopting TDC per pixel, we believe the future lies in moving more “photon processing” onto pixels. Per-pixel histogramming

allows on-chip TCSPC implementations with photon time-event rate approaching the laser excitation rate in every pixel of the array. Moreover it speeds-up the acquisition of time-events by processing them locally while at the same time compressing significantly the time-event transfer to PC for further processing.

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TABLE I
PERFORMANCE SUMMARY OF THE SPAD LINE SENSOR

	Blue SPADs	Red SPADs	Unit
Array Format	1024 × 8		
Chip size	1.990 × 12.648		mm
Pixel pitch	23.78		μm
Fill factor (FF)	49.31	28.20	%
SPAD breakdown voltage (VBD)	14.1	24.6	V
Dark count rate (DCR)	90 (VEB = 1V) 400 (VEB = 1.5V) 1050 (VEB = 3V)	10 (VEB = 1V) 50 (VEB = 1.5V) 200 (VEB = 3V)	Hz
Photon detection probability (PDP)	32 (@480nm, VEB = 1V) 40 (@480nm, VEB = 1.5V)	25 (@620nm, VEB = 1V) 40 (@620nm, VEB = 1.5V)	%
Mean FWHM of IRF	164 @500nm 98 @650nm	237 @500nm 139 @650nm	ps
Mean TDC resolution (1 LSB)	51.2		ps
TDC range	3,355.4 (in TCSPC mode) and 209.9 (in Histogramming mode)		ns
TDC DNL (0 to 50ns)	+0.37/-0.37 (max/min)		LSB
TDC INL (0 to 50ns)	+3.10/-3.96 (max/min)		LSB
Delay range	0 to 516 (in steps of 63ps)		ns
Power consumption with a 33.33 MHz system clock, 20 MHz laser repetition rate, 1.2 V digital core supply voltage (VDD), 3.3 V I/O pads supply voltage (VDDE3V3), 1 V excess bias voltage (VEB), and 3 V SPADs quench voltage (VQUENCH)	SPC mode (with 22bit/pixel) @ 100.2 GS/s: 93.38 core digital & 86.86 I/O pads (Total = 180.24) TCSPC mode (with 11bit/pixel) @ 170.67 MS/s: 80.06 core digital & 165.56 I/O pads (Total = 245.62) Histogramming mode (with 16bin/pixel & 22bit/bin) @ 9.2 GS/s: 133.19 core digital & 34.91 I/O pads (Total = 168.10)		mW
Readout rate @40 MHz system clock	454 (11bit/pixel unchained SPC mode) 227 (22bit/pixel chained SPC mode) 454 (11bit/pixel TCSPC mode) 312 (16bit/pixel TCSPC mode) 14.2 (32bin/pixel & 11bit/bin unchained Histogramming mode) 14.2 (16bin/pixel & 22bit/bin chained Histogramming mode)		klines/s
Readout rate @40 MHz system clock	2560		Mbps

TABLE II
COMPARISON OF CMOS SPAD LINE SENSORS

	Pancheri et al. [2]	Maruyama et al. [4] (type-I & II)	Pavia et al. [39]	Nissinen et al. [40]	Burri et al. [9]	Kufcsak et al. [6]	This work
CMOS process [nm]	350	350	130 (3D)	350	350	130	130
SPAD array size [column × row]	64×4	1024×8	400×1	16×256	256×1	256×4 (Red SPADs) 256×4 (Blue SPADs)	1024×8 (Blue SPADs) 1024×8 (Red SPADs)
Pixel pitch [μm]	26	24	11	35	24	23.78	23.78
FF	34%	4.9%, 44.3%	23.3%	26%	40%	43.7%	49.31% (Blue SPADs) 28.20% (Red SPADs)
Chip size [mm ²]	3.3×3.2	24.7 × 0.8 24.7 × 1.2	5 × 0.77	9 × 3	1.68 × 6.8	0.958 × 6.660	1.990 × 12.648
PDP	32% (@450 nm, VEB = 3V)	34% (@465nm, VEB = 3V)	12.2% (@800nm, VEB = 1.5)		> 25% (@465nm, VEB = 1.5V)		Blue SPADs: 40% (@480nm, VEB = 1.5V) Red SPADs: 40% (@620nm, VEB = 1.5V)
Median DCR [Hz]	1k (typical)	80, 57k (VEB = 3V)	35k (VEB = 1.5V)		2.5k	74.4k (Blue SPADs), 1k (Red SPADs) (VEB = 1.2V)	400 (Blue SPADs), 50 (Red SPADs) (VEB = 1.5V)
# of timing channels	64	1024	100	256	64	256	512
TDC resolution [ps]	160	250	49.7	52	25	426	51.2
IRF (FWHM) [ps]				225		Blue SPADs: 570 @600nm Red SPADs: 620 @600nm	Blue SPADs: 164 (Mean) @500nm Red SPADs: 139 (Mean) @650nm
Output data rate [Mbps]	320		1040	716.8*		209**	2560 @40MHz IO rate
Data compression	none	none	none	none	FPGA Histogramming	On-chip CMM	On-chip Histogramming

*Converted from 400 kframes/s (256 columns and 7-bit/column); **Converted from 19 klines/s (256 columns and 43-bit/column)

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